gating means coupled to [said memory in] a register and said trailing edge circuit connected thereto for reading out data of said timing means when data stored in said memory conforms to [said] a temporal relationship [signal] signaled by said trailing edge circuit and discards data which does not conform to said temporal relationship, transducer means connected to said first and second channels and adapted to receive said first and second signals, and counting means activated by said gating means to count in an up direction in response to a lead signal corresponding to a wave approaching from the right of the axis of said transducer means, and to count down in response to a lag signal corresponding to a wave approaching from the left of said axis of said transducer means.

(C) 2. (Amended) A delay measurement circuit providing a differential delay measurement free of noise induced bias errors comprising:

first and second channels for receiving first and second signals, each of said signals having a leading edge and a trailing edge;

a leading edge circuit coupled to said first and second channels for signaling the temporal relationship of the leading edges of said first and said second signals;

a trailing edge circuit coupled to said first and second channels for signaling the temporal relationship of the trailing edges of said first and second signals;

means for measuring the differential delay between the leading edges of [two] said first and second signals;

means for comparing a temporal relationship of the trailing edges of said [two] first and second signals with a temporal

 